REMARKS

Claims 1-18 will be pending upon entry of the present amendment. Claims 1-6, 10, and 15 have been amended, and new claims 16-18 are herein submitted.

The Examiner has objected to the disclosure under 37 C.F.R. § 1.71, as being incomprehensible. The Examiner cites a line in claim 1, which reads "loading test data and/or instructions into . . .".

Applicant calls the Examiner's attention to the specification, beginning on the first line of page 6, which reads, "where a test program is to be run instead of a standard one, the method of this invention provides for the control logic 4 to read from the external memory rather than from the internal array 2. The input/output pins of the device 1 can be utilized for the purpose.

"For example, the address of the external memory 7 (*i.e.*, the program counter) can be supplied through the data pins 6, while through the address pins 8, the external memory 7 will supply the internal logic with an instruction for decodification and execution by it."

Clearly, the specification provides a clear description of how test data and/or instructions may be loaded into the control logic 4. Accordingly, applicant believes that the disclosure is fully comprehensible to one having ordinary skill in the art.

The Examiner has objected to the drawing under 37 C.F.R. § 1.84(p)(3). Accordingly, a corrected drawing is herewith submitted, including the corrections as required by the Examiner. In addition, the figure has been amended to include a control logic module 12 as part of the test operation control device 9. Support for this amendment may be found in the specification on page 5, beginning at line 15, which reads, "As will be appreciated the test operation control device 9 may also comprise logic circuitry to simulate the control logic 4 . . . ."

The specification has been amended to correct a typographical error, and to provide a reference numeral for the feature added in the drawing. No new matter has been added.

The Examiner has objected to claims 14 and 15 under 37 C.F.R. § 1.126, as being incorrectly numbered. Accordingly, the second claim 14 has been amended to be claim 15 as required by the Examiner.

The Examiner has rejected claims 1-5 under 35 U.S.C. § 112, first paragraph. In particular, the Examiner takes exception to the single step of claim 1, stating that a single step claim is subject to an undue breadth rejection. Accordingly, claim 1 has been amended to incorporate a second step, and is now in condition for allowance.

The Examiner has rejected claims 2-5 under 35 U.S.C. § 112, second paragraph, as being indefinite for not setting forth steps involved in the method/process. Accordingly, claims 2-5 have been amended to recite additional steps.

The Examiner has rejected claims 6-8 under 35 U.S.C. §103(a) as being unpatentable over Mullarkey et al. (US 5,732,033) in view of Bond et al. (US 4,450,559). The Examiner has rejected claims 9-13 under 35 U.S.C. § 103(a) as being unpatentable over Mullarkey in view of Kumakura et al. (US 5,566,386). The Examiner has rejected claims 14 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Kumakura. Claims 1-5 have been rejected as being similar to claims 6-15, and thus subject to the same rejections.

To clarify the issues in question for the Examiner, and to make more understandable the arguments with respect to the rejections, a brief discussion of the general principles of the invention will be made, prior to addressing the rejections specifically.

As the background of the present application explains, control logic circuits are commonly included on memory chips, especially those of the current generation. Inasmuch as testing, both during and upon completion of the manufacturing process, is required, a common of testing such chips is to provide circuits onboard the same chip for that purpose. For example, the Mullarkey reference cited by the Examiner in the present Office Action teaches the formation of circuitry dedicated to such testing onboard. (See, for example, column 2, lines 17-26, 34-36, and 44-48.)

As explained on page 3 of the present application, beginning at Line 2, "A drawback with the above testing method is that complex gates must be included in the design of the control logic portion devoted to testing, which expands the area requirements of the device to a considerable extent.

"A commonly adopted solution consists of testing only the analog circuitry . . . . Where the operability of the various parts of the control logic are to be tested in situations other

than those provided by the algorithm, a certain number of test registers are included which are effective to drive the analog circuits, once suitably loaded. Again, the overall area for occupation by the circuit must be expanded, merely to enable the testing operations to be performed."

According to an embodiment of the invention, and as illustrated in the Figure, a control device 9 is provided, which includes a feature for testing the integrated circuit 1. For example, as described in the present application beginning on page 4, line 21, "The control device 9 may be an external memory array 7 . . . substantially like that incorporated in the device 1. In another embodiment, the control device 9 may be a control logic 12 substantially like that incorporated in the device 1."

Operation of the device is described in the current specification as follows: "Accordingly to the principles of the invention the external array 7 is used to simulate the internal memory 2, making possible the direct test and observation of the interaction of the control logic 4 with the array 7." (See page 5, lines 9-12.)

It will be appreciated that in a conventional system, such as that described with reference to the Mullarkey reference, interaction between the logic circuitry on a chip and the test circuitry provided on the same chip cannot be directly observed. Furthermore, errors detected in such testing cannot be immediately attributed to the logic circuitry, inasmuch as such errors may originate in failures of the test circuitry itself.

The operation of the system is further described in the present application as follows: "As will be appreciated, the test operation control device 9 may also comprise logic circuitry 12 to simulate the control logic 4, for the purpose of testing and observing the memory array 2 directly, and in isolation from the control logic 4.

"Thus, the invention is advantageous especially in that it allows the control algorithm of circuit portions of the memory device 1 to be changed in order to carry out a series of different tests. This not only allows the circuit portions of the device 1 to be controlled as desired, but also the control logic 4 itself to be isolated and tested for operability in a self-diagnosis mode.

"These are not features that a conventional microprogrammed unit can possibly offer because its code storing array would be substantially unchangeable . . . ." (Page 5, lines 15-28.)

Amended claim 6 recites, in part, "the control device comprising a memory unit external of and detachably connectable to the memory device, the memory unit configured to operate in substitution of the memory cell array during testing."

Mullarkey in combination with Bond fails to teach a memory unit configured to operate in substitution of a memory cell array during testing. In contrast, Mullarkey teaches the formation of a plurality of pass gates disposed in a spare memory array for the purpose of testing the device, thus teaching away from the device claimed in claim 6 (column 2, lines 19-48).

For its part, Bond teaches the provision of spare memory to function as permanent replacement for defective cells in a memory device. However, Bond provides no instructions as to how a memory should be tested, or defective cells located.

Bond states, "assume that a diagnostic check was made of each of the word addresses in main memory and that at each word address, each of the defective cells was identified. For purposes of explanation it will be assumed that . . . only those chips in rows 1-4 may have defects." (Column 7, lines 53-60.)

Clearly, Bond does not envision the use of spare cells for the purpose of testing a memory, but only for replacing defective cells once they have been identified by a test. Accordingly, there is no motivation to combine the external cells of Bond with the testing device of Mullarkey.

The Examiner states, "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Mullarkey with the teaching of Bond by simply using one memory and second memory as external, because one of ordinary skill in the art would simply use an external memory for the test of the memory into integrated circuit to provide minimization of the integrated circuit (IC) dimensions, universality of application, and convenience for the test equipment."

Applicant respectfully traverses this position, noting that none of the art cited by the Examiner suggests the use of an external memory array as a substitution for an array on a

memory chip to test the logic on that same chip. Mullarkey teaches away from this concept, while Bond offers no suggestion as to how a logic circuit or memory array should be tested. Applicant believes that such a concept is obvious only in light of the present application. Accordingly, claim 6 is allowable over the cited prior art, together with dependent claims 7 and 8.

Claim 9 recites, in part, "a test control device, external to the semiconductor substrate, having a circuit for simulating the internal memory array to permit testing of the control logic circuit in isolation from the internal memory array."

In rejecting claim 9, the Examiner has cited Mullarkey in combination with Kumakura as teaching the limitations thereof. The Examiner acknowledges that Mullarkey does not explicitly teach or point out the external test control. In fact, Mullarkey specifically teaches an internal test circuit, as previously described. For its part, Kumakura teaches also the formation of internal circuitry for the purpose of testing. For example, Kumakura states, "the nonvolatile semiconductor memory being characterized by the provision of dummy cells provided outside the address of the memory cell matrix . . ."

These dummy cells 20 are illustrated in Figure 4, which is a block diagram showing the configuration of a flash memory accordingly to Kumakura. Figure 4 shows the test dummy cells 20 integrated into the same device with a flash memory cell matrix 17. Kumakura regards the placement of the dummy circuits and testing circuitry on the memory device as being advantageous, and offers no suggestion that they might be formed separate from the memory device. Accordingly, a combination of Kumakura with Mullarkey does not anticipate or suggest the limitations of claim 9. Claim 9, therefore, is allowable over the cited prior art. Dependent claims 10-13 are also allowable thereover.

In rejecting claim 14, the Examiner has cited Kumakura as teaching or suggesting the limitations thereof. The Examiner lists several features considered relevant, and states, "Kumakura does not explicitly teach and point out to the external location of any or some means . . ."

In fact, Kumakura teaches explicitly the internal location of all of the features cited by the Examiner, including the erasure source control circuit 18, the control circuit 16, test

dummy cells 20 and memory array 12. Applicant calls Examiner's attention to Figures 4 and 8, and to lines 61 and 62 of column 7, which indicates that Figure 4 is a block diagram showing the configuration of a flash memory, and column 9, lines 13-15, which indicate that Figure 8 is a detailed view of some of the features of Figure 4. All of the features cited by the Examiner are found in figure 4 or Figure 8, and are thus part of Kumakura's flash memory device, rather than external to it. Accordingly, Kumakura does not teach or suggest the use of an external circuit to simulate the control logic circuit of a memory device as recited in claim 14.

The Examiner states that it would have been "obvious to one having ordinary skill in the art at the time the invention was made to modify Kumakura with the teaching of by using the external locations of any/some means for memory test, because it is obvious and well known, that the procedure for most tests and particularly for memory test control apparatus includes steps of simulating the circuits."

Applicant respectfully disagrees with this position. As has been demonstrated, Kumakura teaches the use of test circuitry formed on the memory device, and offers no suggestion that some portions of that device be simulated, using external circuitry. Applicant respectfully requests that the Examiner provide other evidence beyond the mere statement that it is obvious and well known to simulate a logic circuit, for the purpose of testing a memory array, especially in light of the fact that Kumakura explicitly teaches against such a method. In the absence of such evidence, applicant asserts that claim 14 is allowable over Kumakura.

The Examiner has rejected claim 15 using arguments similar to those used in rejecting claim 14. While the scope of claim 15 differs from that of claim 14, the arguments in support of the allowability of claim 14 may also be applied with reference to claim 15, noting however that while claim 14 is directed to the testing of a memory array, claim 15 is directed to the testing of a control logic circuit. Nevertheless, Kumakura fails again to provide teaching or suggestion justifying rejection of claim 15. In particular, Kumakura teaches the formation of test circuits with the memory array, and fails to suggest or teach an external circuit configured to simulate the memory array, for the purpose of testing the control logic circuit. Accordingly, claim 15 is allowable over Kumakura.

New claims 16-18 are submitted to provide claim protection for features of the invention previously unclaimed. Support for these new claims may be found in the specification beginning on page 6, line 5.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative at (206) 622-4900 in order to expeditiously resolve prosecution of this application.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

Harold H. Bennett II
Registration No. 52,404

HHB:wt
Enclosure:
Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031
433868_1.DOC